Abstract

A structure for flash memory cells with improved endurance characteristics is disclosed. Isolation regions are formed in a semiconductor region separating cells and also separating programming bit line channel regions of a cell from reading bit line channel regions of a cell. A conductive floating gates has a first portion in the programming bit line channel region of a cell and a second portion in the reading bit line channel region of the cell and a third connecting portion passing over an isolation region. A conductive control gate is separated from the floating gate by an intergate insulator layer and has a first portion entirely disposed over the first floating gate portion, where the first floating gate portion completely covers the space between a source region and a drain region, a second portion disposed over the second floating gate portion, where the second floating gate portion does not extend all the way from a source region to a drain region, the second control gate portion completing the covering of the space between a source region and a drain region and a third connecting portion disposed over the third floating gate portion. A programming bit line channel contact line and a reading bit line channel contact line are disposed over a covering insulator layer and connect to drain regions through the covering insulator layer.